JAPANESE PATENT OFFICE

PATENT JOURNAL

KOKAI PATENT APPLICATION NO. HEI 6[1994]-150031

Technical Disclosure Section

Int. Cl.[5]: G 06 F 15/78
12/08
G 11 C 11/34
H 01 L 25/08
G 11 C 11/401
H 01 L 25/065
25/07
25/18

Sequence Nos. for Office Use: Z 7323-5L
G 7323-5L
Z 7608-5B
6741-5L

Application No.: Hei 4[1992]-316614

Application Date: October 30, 1992

Publication Date: May 31, 1994

No. of Claims: 6 (Total of 5 pages)

Examination Request: Not requested

# CPU MODULE

Inventor: Koichi Takemura
NEC Corporation
5-7-1 Shiba, Minato-ku,
Tokyo

Applicant: 000004237
NEC Corporation
5-7-1 Shiba, Minato-ku,
Tokyo

Agent: Naka Sugano, patent attorney

[There are no amendments to this patent.]

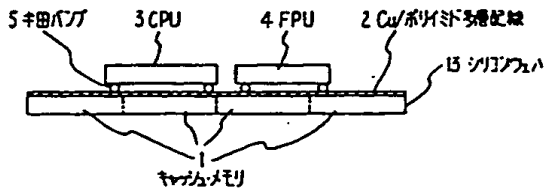
Abstract

Objectives

To provide a small-scale and high-density CPU module with a large cache capacity corresponding to a high-speed operation in a CPU module containing at least a microprocessor and a cache memory.

Constitution

CPU 3, FPU 4, etc., which are packaged, are three-dimensionally arranged via a multilayer wiring 2 using a low-permittivity material as an insulating layer on a cache memory 1, which is not packaged, and the module is housed in one package.



Key: 1 Cache memory
2 Cu/polyimide multilayer record
5 Solder bump
13 Silicon wafer

Claims

1. A CPU module characterized by the fact that in a CPU module having a substrate and a microprocessor, the substrate is a silicon wafer in which a cache memory is housed; and characterized in that the microprocessor includes at least a CPU (central processing unit) and a FPU (floating-point arithmetic processing unit), is mounted at an active layer of the substrate via a wiring, and is electrically connected to the cache memory in the substrate.

2. A CPU module characterized by the fact that in a CPU module having a substrate and a microprocessor, the substrate is formed by integrating several semiconductor chips containing at least a cache memory chip and another base material; and characterized in that the microprocessor includes at least a CPU (central processing unit) and a FPU (floating-point arithmetic processing unit), is mounted at an active layer of the substrate via a wiring, and is electrically connected to the cache memory in the substrate.

3. A CPU module characterized by the fact that in a CPU module having the CPU of Claim 1 or 2, the above-mentioned wiring for connecting the cache memory and the processor is obtained by cutting part of the inside of the same wiring layer and electrically cutting off an optional cache memory in the substrate from the processor.

4. A CPU module characterized by the fact that in a CPU module having the CPU of Claim 1 or 2, the above-mentioned wiring for connecting the cache memory and the processor is obtained by selectively connecting part of it and electrically connecting the cache memory and the processor in the substrate without being connected in advance in the same wiring layer.

5. A CPU module characterized by the fact that in a CPU module having the CPU of Claims 1, 2, 3, or 4, the above-mentioned wiring for connecting the cache memory and the processor is a multilayer wiring in which a wiring layer, composed of Cu or Au or Al and Al-Si alloy as a main conductive layer, and an insulating layer of a polyimide or a polymer with a permittivity of 4 or less are laminated in a multilayer shape.

6. A CPU module characterized by the fact that in a CPU module having the CPU of Claims 1, 2, 3, 4, or 5, the above-mentioned cache memory housed or integrated in the substrate is a nonvolatile memory utilizing the polarization inversion of a ferroelectric.

* * *